Application Serial No.	:	10/667,021
Filed	:	18 September 2003
Applicant	:	R. Moss et al.
Title	:	METHODS AND STRUCTURE FOR SCAN TESTING OF SECURE SYSTEMS
Art Unit	:	2136
Examiner	:	E. Shiferaw
Docket Number	:	03-0172
Date	:	9 October 2008

TELEPHONE INTERVIEW SUMMARY

Applicant submits this telephone interview summary to meet the requirements of 37 C.F.R. § 1.133(b), and according to the requirements listed in MPEP § 713.04.

Date/Type of Interview: telephone interview conducted on 7-8 October 2008

Examiner: E. Shiferaw

Name of Applicant's attorney: Dan Fishman

Exhibits shown or demonstrations conducted: None

Claims discussed: 1

Prior art discussed: None

General thrust of Examiner's arguments: see below

General thrust of Applicant's arguments: see below

Agreement reached and general nature of the agreement: see below

Proposed amendments: None

The undersigned attorney contacted the Examiner regarding the office action mailed 9 July 2008 in which the Examiner essentially repeated the prior §103 rejections and added a new rejection under §101 (applied to various claims including, for example, claim 1). The Examiner in essence states that the claim does not recite any "hardware" (and thus not a "machine" under §101) but only "software" and further states that software, per se, is not patentable subject matter. The Examiner points to a portion of the specification on pages 7 and 8 that describe "logic" that receives and generates signals presented on figure 4. Figure 4 is a timing diagram of those signals received and

generated by the logic elements of the claimed integrated circuit. The Examiner suggests that the word "logic" used in the cited portion of the specification is understood to mean "software".

The undersigned attorney expressed strong disagreement with the Examiner's presentation of, and support for, the §101 rejection. To interpret "logic" as meaning "software" in the context of the specification and claims that are clearly reciting features in an integrated circuit is wholly unreasonable and totally inconsistent with the plain meaning to those of ordinary skill in the art. Perhaps the Examiner's Computer Science background (as distinct from an Electrical Engineering background) explains such a gross misinterpretation. Nothing in the subject application (claims or specification) remotely suggests that the invention is a software invention. Even if it did, the undersigned attorney takes strong issue with such broad statements as "software is not patentable". Regardless, the claims and the supporting specification are clearly reciting hardware elements - namely, an integrated circuit comprising particular, clearly recited, logic elements - clearly not software and clearly patentable subject matter.

However, in hopes of advancing prosecution, the Examiner seemed to agree with the undersigned attorney that if the preamble (e.g., of claim 1) were altered to read: "An integrated circuit having scan test features ~~and including~~, the integrated circuit comprising:" that she may more clearly understand the invention to be a circuit with specific recited functional logic elements. However, the Examiner seemed reluctant to agree to any specific amendatory language

The undersigned attorney also expressed the desire to discuss the substance of the §103 rejections. The Examiner responded that she was not prepared to discuss the §103 rejection in substance but instead scheduled another conference for later this month.

Date: 9 October 2008

/Daniel N. Fishman/
SIGNATURE OF PRACTITIONER

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